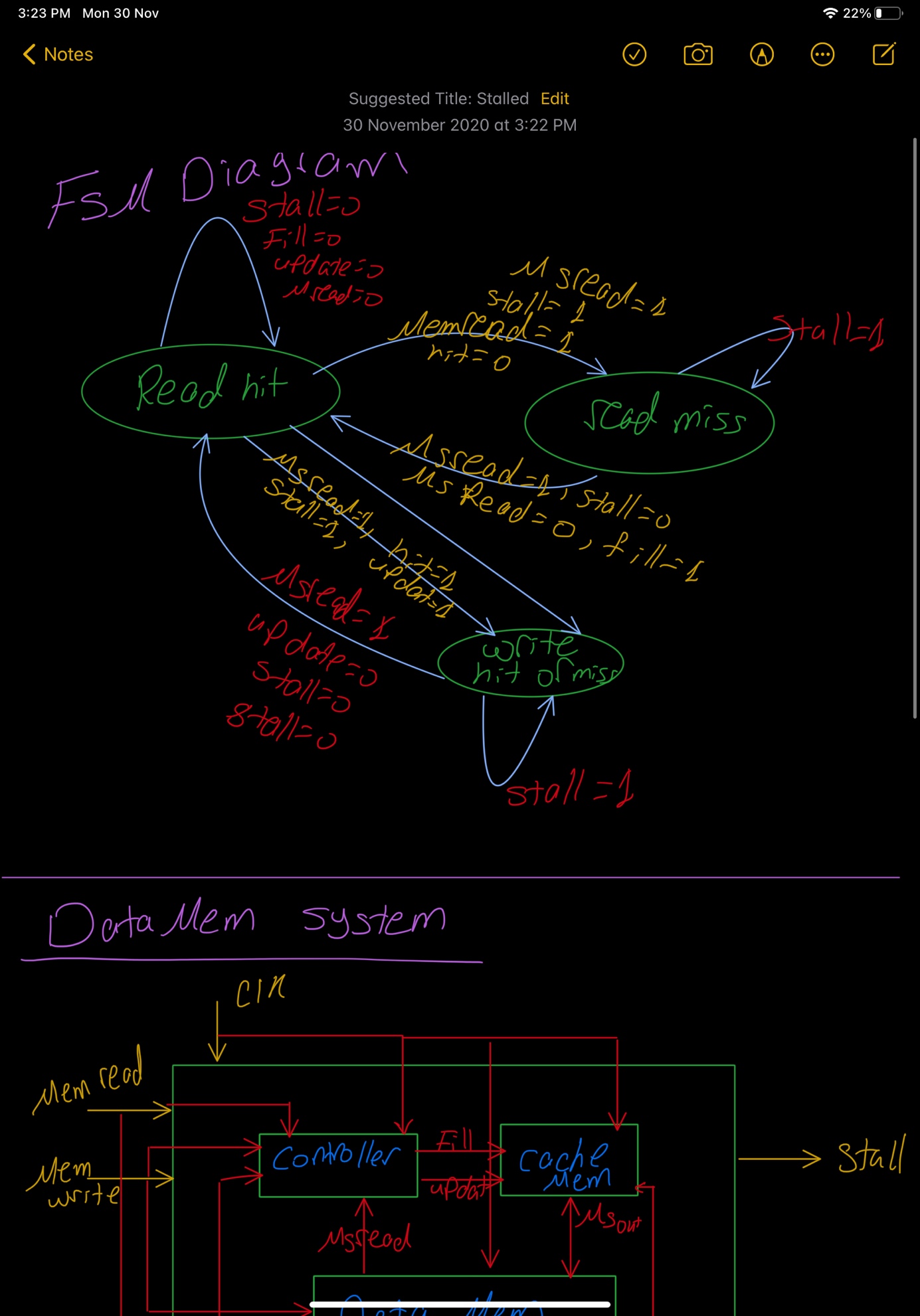
Lab 10

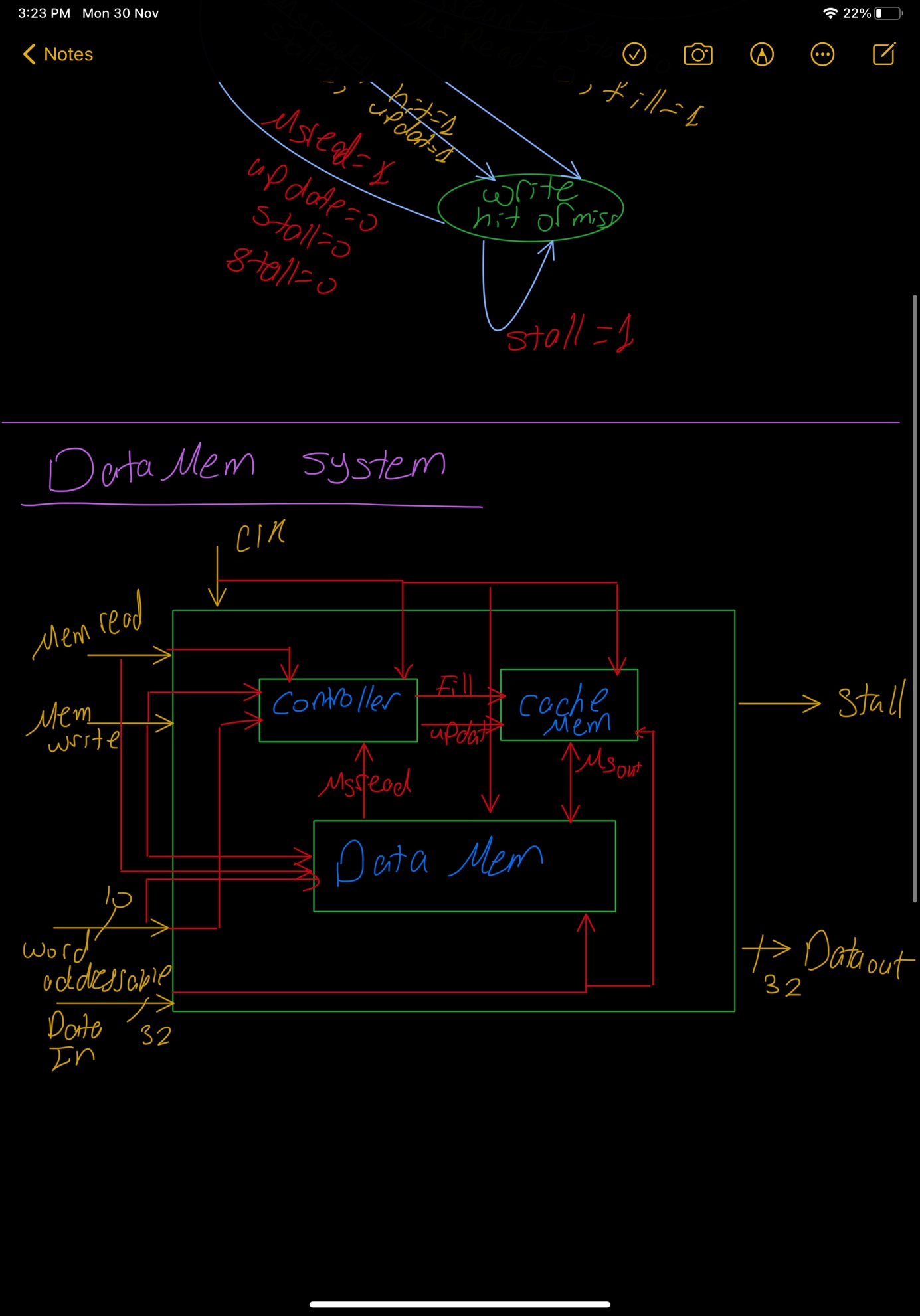
Experiment 3:

We did the cache controller



Experiment 4:

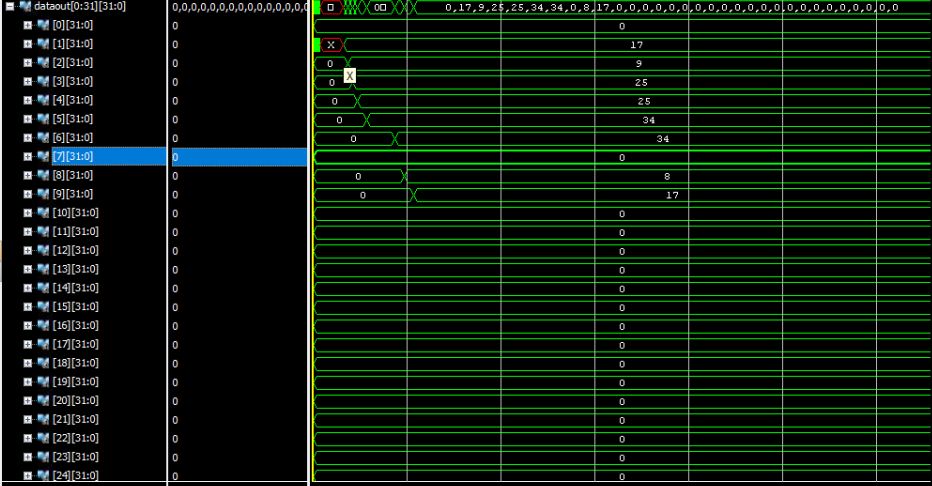
We did the data system memory module



ScreenShots for simulation:

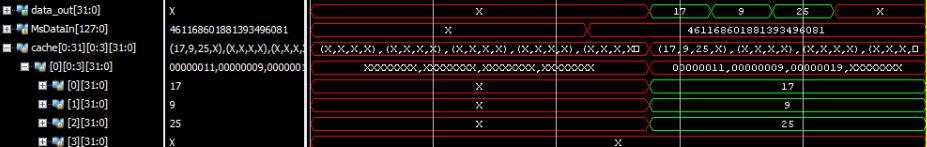
1)

These are the register file

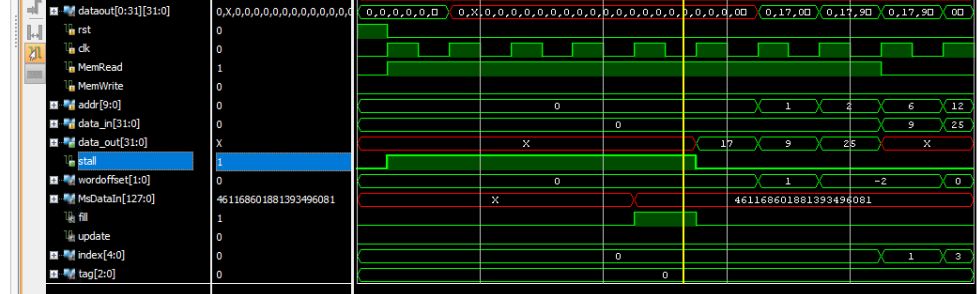


2)

There are the cache



3) This is the stall signal and the PC results



4)

